The course will cover an overview of electronic testing, automated model generation for high level fault modeling (HLFM), system level testing for complex system-on-chips including design-for-testability and core-based test scheduling. The topics of logic built-in self-test (LBIST) will also be covered, with an example LBIST implementation case study looking at several low power techniques. Participants will get an opportunity to have hands-on experience on high-level automated model generation using software provided from Mentor Graphics.

**Targeted Audience:** The one-day short course targets to Electronic engineers, Researchers, Postgraduate Students, and Industry Researchers

**Facilitators**

**Dr Fawnizu Azmadi Hussin** is an Associate Professor at the Universiti Teknologi PETRONAS (UTP), Malaysia. He was the program manager of Master by coursework program at UTP (2009-2013) and the Deputy Head of Electrical & Electronic Engineering department at UTP since 2013. He obtained the Bachelor of Electrical Engineering (Computer Design) from the University of Minnesota, Twin Cities, U.S.A. in 1999 and subsequently his M.Eng.Sc. in Systems and Control from the University of New South Wales, Australia in 2001. Dr Fawnizu completed his PhD in 2008 at the Nara Institute of Science and Technology in Japan under the scholarship from the Japanese Government (Monbukagakusho). His PhD thesis was on core-based testing of system-on-chips (SOC) and network-on-chips (NOC), which won an award ASP-DAC 2008 Student Forum. Dr Fawnizu’s research interests are in VLSI design and test especially in core-based testing, SOC and NOC. Dr Fawnizu currently works on functional debug of integrated circuits and on test program generation for software-based self-test. He is actively involved with the IEEE Malaysia Section. He is the 2013 Chair of the IEEE Circuits and Systems Society Malaysia Chapter.

**Dr. Likun Xia** Received his MSc degree from the University of Newcastle, UK in September 2001, and PhD in 2009 in VLSI Design and Test Group at the University of Hull, UK. He is currently a senior Lecturer/Researcher at Electrical & Electronic Engineering Department, Universiti Teknologi PETRONAS (UTP), Malaysia. He is a member of IEEE CAS and EAGE. He is interested in mathematical behaviour modelling for various applications including high level fault modeling for analogue and mixed-signal circuit and system; biomarker development in Neuroscience on stress and depression issues; and seismic imaging on fractured reservoir.

He has published various publications in top-tier journals including IEEE TCAD, JETTA, and also attended international conferences such as ISCAS, EMBC, and ASP-DAC.

**For Any Further Information, Please contact**

Mr. Dileep Kumar (Research Scientist), CISIR, UTP, Email: dileep.utp@gmail.com
Phone: 0195591650

**Venue:**
Centre for Intelligent Signal and Imaging Research (CISIR)
Universiti Teknologi PETRONAS
Bandar Seri Iskandar, Tronoh
31750, Perak, Malaysia

**Organized By:**
Centre for Intelligent Signal and Imaging Research (CISIR)
Universiti Teknologi PETRONAS
Bandar Seri Iskandar, Tronoh
31750, Perak, Malaysia
Programme Schedule

Day 1:

08:00  Registration & Opening Remarks
09:00  Review of Automated Model Generation Approaches for High Level Fault Modeling in Analogue and Mixed-Signal Systems
10:30  Tea break
11:00  Practical session: Performing of High level modelling and high level fault modelling using Mentor Graphics software
12:30  Lunch Break
14:00  Introduction to SOC testing
       Challenges in SOC testing
       Motivation for modular testing of SOCs
       Test wrapper design and optimization
       Test access mechanism design and optimization
15:30  Tea break
16:00  Test scheduling
       IEEE 1500 core test standard
       Built-in Self-test for complex SOC
17:00  Adjourn

For On-line transaction and cash deposit to ITP account, please use the account information below

INSTITUTE OF TEKNOLOGI PETRONAS SDN BHD (352875-U):
0809-0004124-054 (CIMB Bank Berhad, Batu Gajah)

Kindly fill the registration form and send a scan copy of filled form to one of the below e-mails:
dileep.utp@gmail.com or cisirutp@gmail.com

Note:— Registration should be completed 4 days before course commencement. First-come, first-served policy is implemented due to limited seats

Accommodation

Participants are required to make their own arrangements for accommodation near by Venue.

For Any Further Information, Please contact

Mr. Dileep Kumar (Research Scientist)
Centre for Intelligent Signal and Imaging (CISIR),
Universiti Teknologi Petronas, Malaysia
dileep.utp@gmail.com or dileep.kumar@petronas.com.my
Phone/Mobile : 0195591650

Fees for Participants from Malaysian Universities

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<th>Price</th>
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<tr>
<td>IEEE Student Member/Full IEEE CAS Member</td>
<td>RM 650</td>
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<tr>
<td>Student Non-Member</td>
<td>RM 700</td>
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<tr>
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<td>RM 750</td>
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</table>

The fee is per person and includes lunch, refreshments and short course materials only. A certificate of attendance will be given at the end of the course. Participants are required to bring their own Laptop.

Objectives

- To introduce basic difficulty faced by semiconductor industries and the concepts of faults in analogues and/or digital circuits and systems
- To explain various types of fault-free and faulty models for analogues and mixed circuits and systems
- To compare the benefits of modular testing against conventional monolithic testing
- To apply the concept of modular test methodology for complex system-on-chip (SOC)
- To explore the use of logic BIST for testing of complex SOC

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