Probabilistic Neural Computing with Nanoscale CMOS

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Content

• Motivation
• Brief intro on probabilistic neural computing
• Neural hardware
• Research activities
Probabilistic Neural Computing with nanoCMOS

Silicon MOSFET scaling

1990s: Golden era
- Gate oxide thickness scaling
- Junction scaling
- Vcc scaling

Limiter:
- Gate oxide tunnelling
- Mobility degradation

Innovations:
- Strain engineering (introduced at 90nm)
- High-κ gate insulator (introduced at 45nm)
- Metal gate (introduced at 45nm)

0.7x every 2 years

1000
100
112.5 nm
1995 2000 2005 2010

Gate Pitch (nm) 0.7x every 2 years

P. Packan et al, IEDM2009

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Variability in 65nm (L=65nm, W=140nm)

T. Hiramoto (Tokyo Univ.)
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Variability in 65nm (L=65nm, W=140nm)

Systematic components
Random components

Original distribution data

T. Hiramoto (Tokyo Univ.)

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Tsunomura, Nishida, Hiramoto, JJAP, 2009
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**Static Statistical Variability**

A. Asenov (Glasgow Univ.)

- Random dopants
- Polysilicon/high-k granularity
- Line edge roughness

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**Dynamic Statistical Variability**

A. Asenov (Glasgow Univ.)

- Continuous
- Single trap
- Multiple traps

Threshold voltage shift

Probability

$\Delta V = \Delta \Delta V$

$N_D = 1 \times 10^{11}$
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Challenge in IC design

- Normalised Energy per Cycle (a.u.)
- Normalised Circuit Delay (a.u.)

22nm

T0

After 3 yrs

Alternative solutions

- Redundant circuits
  - Array-based architecture with CNT/SNW
  - NanoFabric with NDR latches
    [Stan et al, Proc. IEEE, 2003]
  - von Neumann multiplexing

- Neural networks
  - CMOL CrossNets
    [Likharev, Stony Brook Univ.]
  - Markov Random Fields
    [Bahar, Mundy and Chen, ICCAD, 2003]

Nanoarray (DeHon, 2003)
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Probabilistic Neural Computing

- First developed by Specht in late 1980s
  \[ P(m | e) = \frac{P(e | m)P(m)}{P(e)} \]
  - Map any input pattern to a number of classifications
  - Can be forced into a more general function approximator
  - Applied to radar image processing, stock trend prediction, abnormal heartbeat detection, electrochemical sensor fusion.

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Probabilistic Neural Computing in hardware

Silicon Cochlear

CRBM

eNose

Silicon Retina
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Research Activities

• Integrating RTS noise into circuit analysis

• Probabilistic neural computing (CRBM) with noisy circuits

• Statistical NBTI-effect prediction for ULSI circuits

• Modeling 1/f noise for sub-45

• Neuromorphic engineering
  • E-nose, e-tongue
  • RPO transistor as noisy neurons
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Possible collaboration

- Noise/device degradation modeling for CMOS
- Probabilistic neural computing (algorithm/hardware)
- Application (sensor system)

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